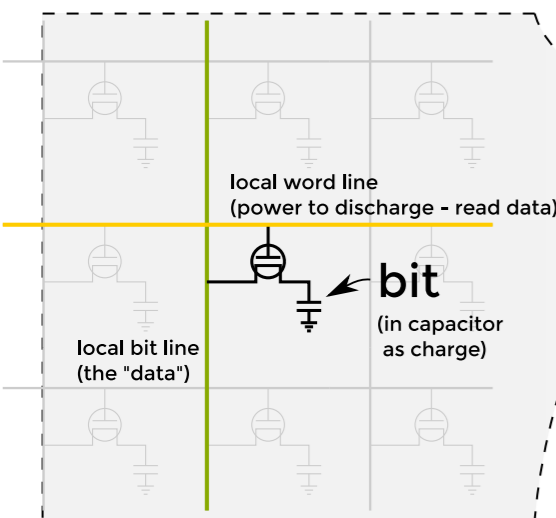


RAM Anatomy Poster

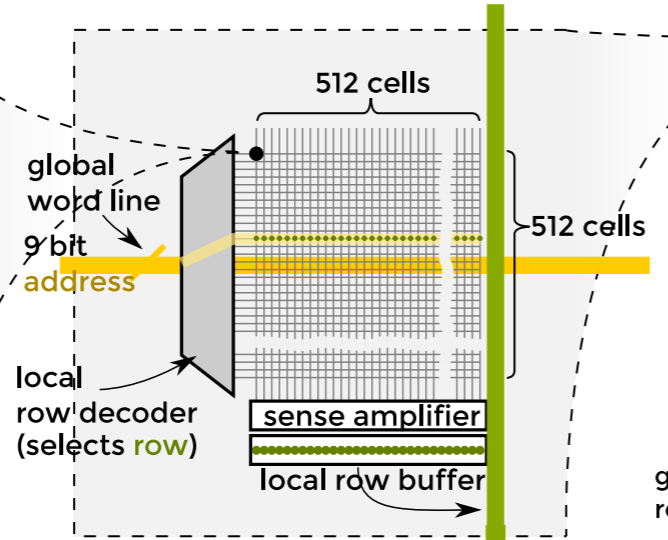
SDRAM 8GB DDR4 CL8-8-8-24^(*)



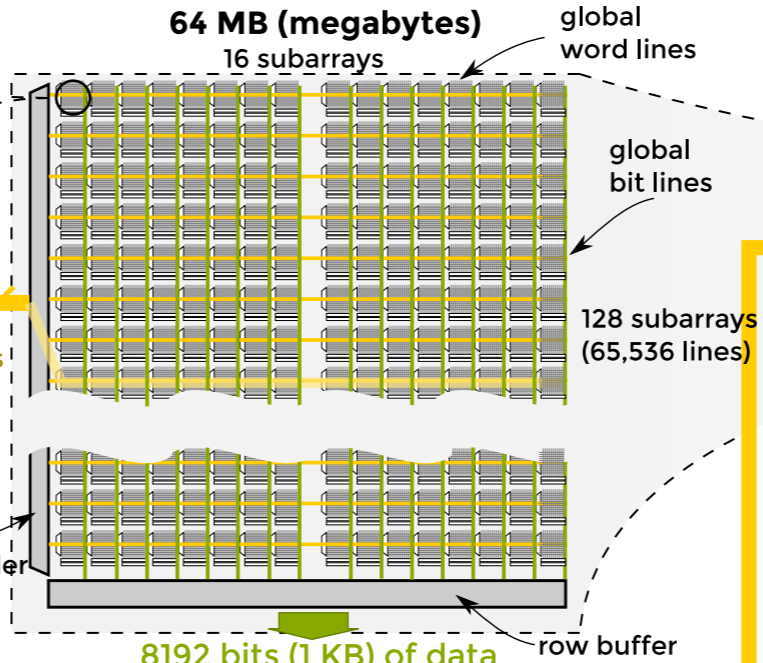
Single DRAM cell 1 bit



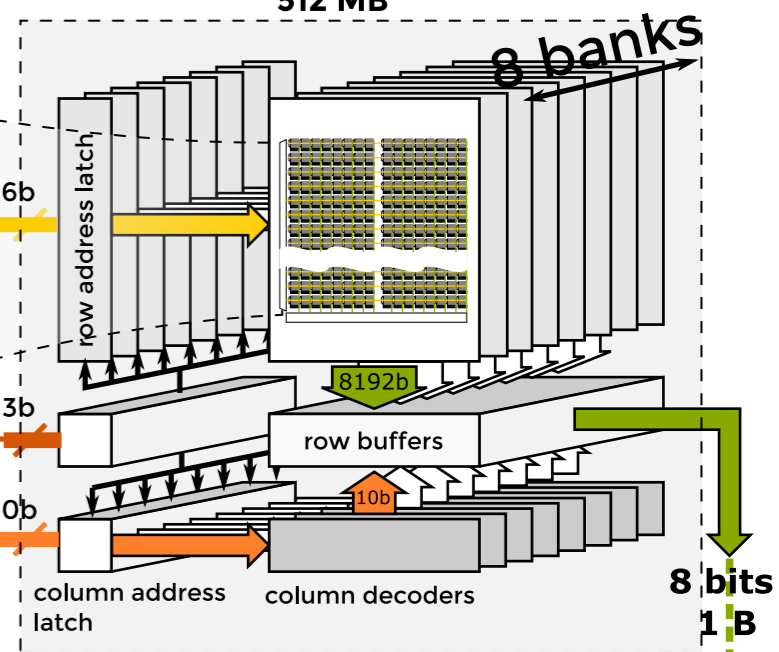
subarray (SA) 32 KB (kilobytes)



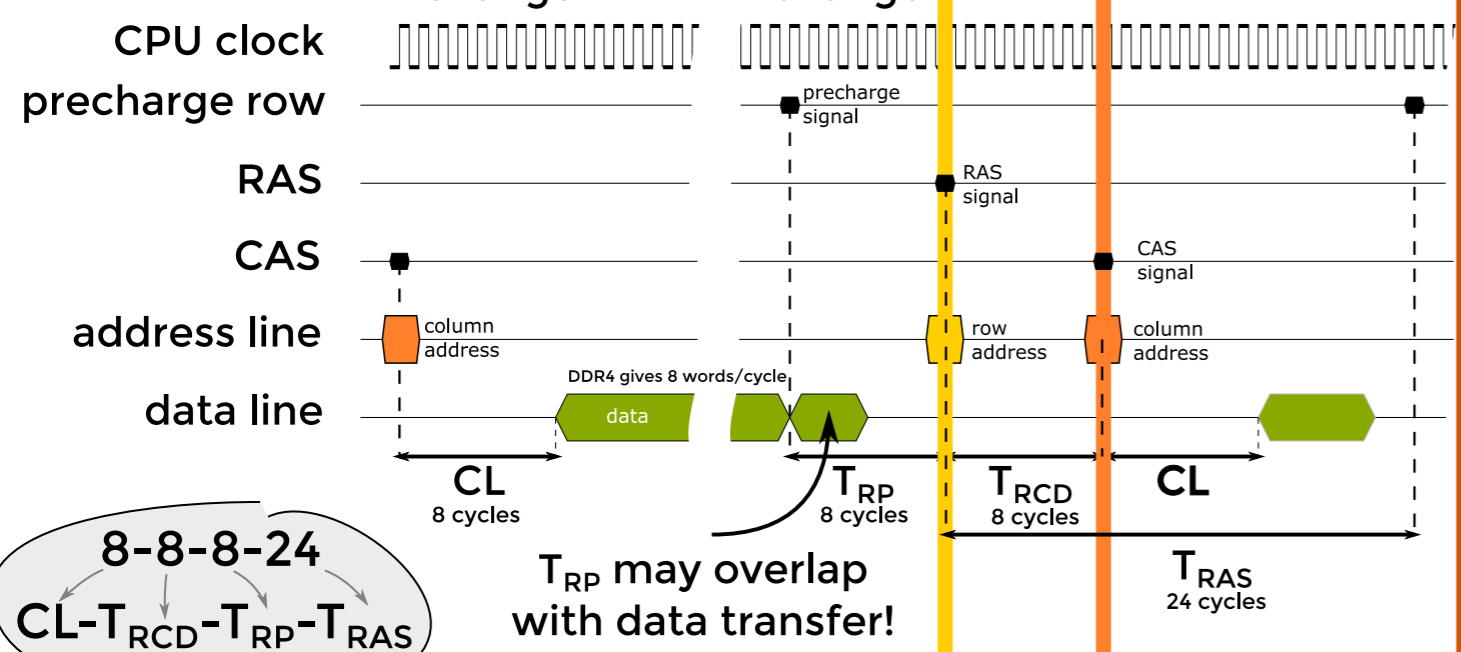
bank 64 MB (megabytes)



Single DRAM chip 512 MB

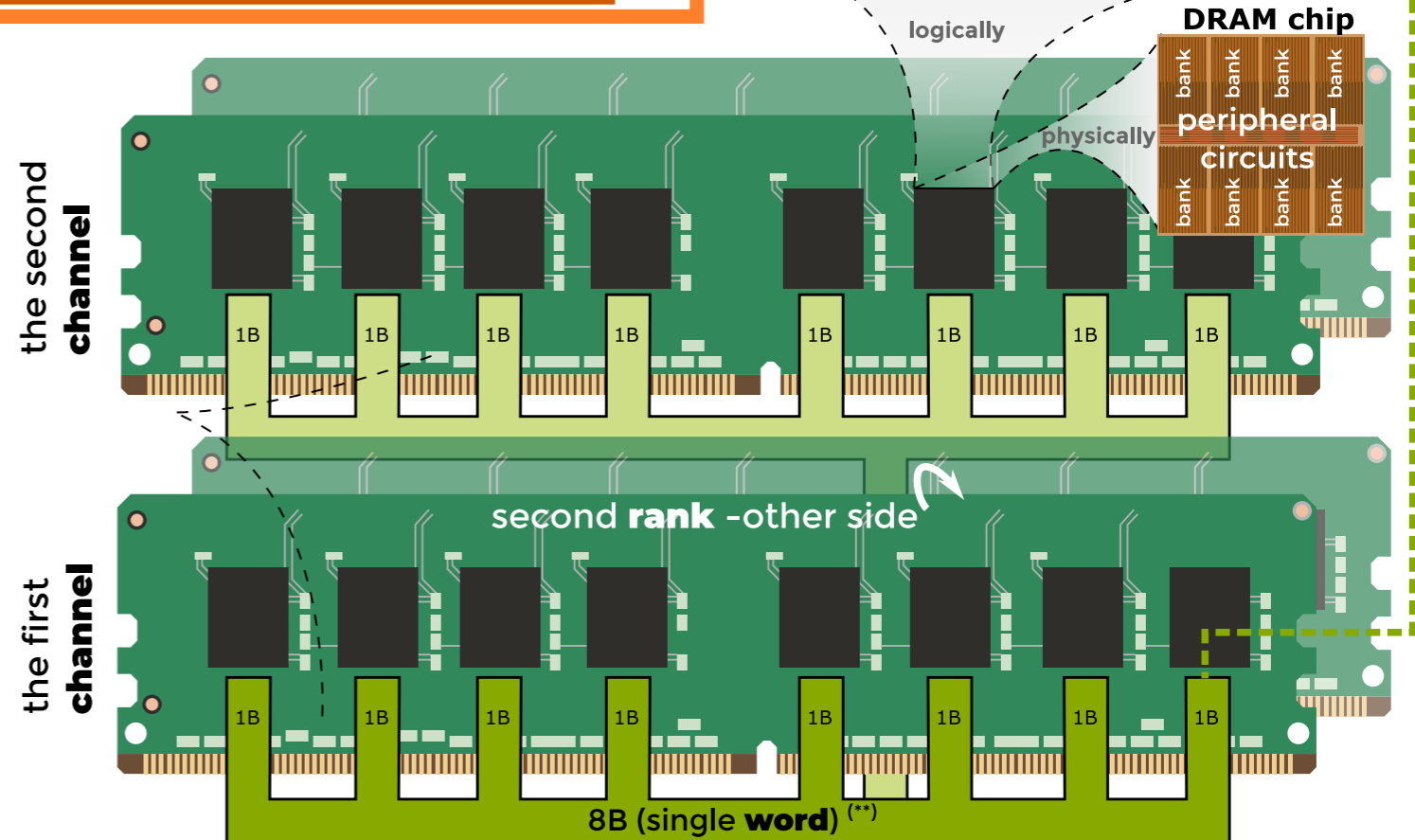
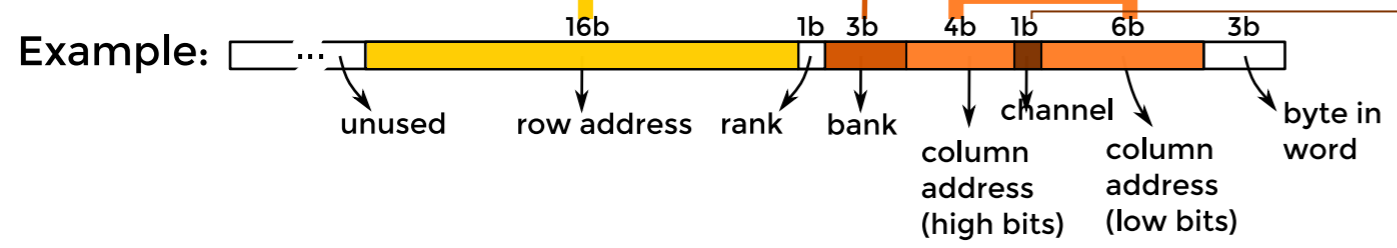


Timings



8-8-8-24
CL-TRCD-TRP-TRAS

Physical address



Memory controller

^(*) sample 8GB SDRAM module - 2 ranks with 8 DRAM chips (512MB each - consist of 8 banks, 64MB each). Internal structures are simplified for illustratory purposes and may differ in various modules

^(**) In case of DDR4 it is multiplied by eight, so 8 words/CPU cycle